

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-2. (canceled)

3. (original) A method comprising:

separating a random number generator into a single first stage and a second stage;

replicating the circuitry of said second stage into M parallel modules; and

generating M random number outputs using said single first stage circuitry and M

parallel second stage modules,

wherein each of said M modules has a first input which is the output result of said

single first stage circuitry and a second input which is unique to said module,

~~according to claim 2~~ wherein said first stage circuitry has at least two first stage

inputs, a first first stage input representing the integer coordinate components of ~~the~~ a location of

interest and a second first stage input representing ~~the~~ a hardware cycle.

4. (original) A method according to claim 3 wherein generating includes:

storing said first stage inputs in a first register;

selecting a first set of bits from said first register;

storing said first set of bits in a second register; and

selecting a second set of bits from said second register, said second set of bits

representing said result of said single first stage circuitry.

5. (original) A method according to claim 4 wherein for each parallel second

stage module, generating further includes:

storing said result of said single stage circuitry in a second stage register; and

selecting a second set of bits from said second stage register, said second set of

bits representing one of said M random number outputs.

1 6. (currently amended) A method according to claim 5 wherein said each
2 random number output ~~can be~~ is one of a phase 1 output ~~and or~~ a phase 2 output.

1 7. (original) A method according to claim 6 wherein said phase 2 output is a
2 full and exact representation of the desired random number output.

1 8. (original) A method according to claim 7 wherein said phase 1 output is
2 an approximation of said phase 2 output.

1 9. (original) A method according to claim 4 wherein selecting said first set
2 of bits includes:
3 utilizing a group of XORs, each XOR having its inputs pre-wired to various
4 locations of said first register, to select among the bits of said inputs.

1 10. (original) A method according to claim 4 wherein selecting said second
2 set of bits includes:
3 utilizing a group of XORs, each XOR having its inputs pre-wired to various
4 locations of said second register, to select among the bits stored therein.

1 11. (original) A method according to claim 5 wherein said selecting in each
2 parallel second stage module includes:
3 utilizing a group of XORs, each XOR having its inputs wired to a number of bits
4 representing the module number and to selected locations of said second stage register.

1 12. (original) A method according to claim 11 wherein the wired number of
2 bits representing the module number varies from XOR to XOR.

1 13. (original) A method according to claim 11 wherein each parallel second
2 stage module wires its XORs to its registers in an identical manner with all other parallel second
3 stage modules.

14. (canceled)

1 15. (currently amended) An apparatus configured to generate M random
2 number outputs on a given cycle j in a parallel fashion comprising:
3 first stage circuitry configured to accept a series of inputs; and
4 M second stage modules, the output of said first stage wired as an input of each of
5 said M modules, the output of each module being one of said M random number outputs,
6 ~~according to claim 14~~ wherein said series of inputs includes the cycle number j,
7 the number of dimensions desired and integer coordinate components for each dimension
8 desired.

1 16. (currently amended) An apparatus according to claim [[14]] 15 wherein
2 each said second stage module also includes an input k representing the number of the module.

1 17. (original) An apparatus according to claim 15 each said random number
2 output contains a fractional coordinate component for each desired dimension as well as a weight
3 of the corresponding pulse at the location given said fractional coordinate components and said
4 integer coordinate components.

1 18. (currently amended) An apparatus according to claim [[14]] 15 wherein
2 said first stage circuitry comprises:
3 a first register having locations storing each bit of said series of inputs; and
4 a first bank of XORs, each input of each said XOR of said first bank coupled to an
5 arbitrary one of said locations of said first register.

1 19. (original) An apparatus according to claim 18 wherein said first stage
2 circuitry further comprises:
3 a second register having locations storing each output of said first bank of XORs;
4 and
5 a second bank of XORs, each input of said XORs of said second bank coupled to
6 an arbitrary one of said locations of said second register, each output of said second bank of
7 XORs representing each bit of said output of said second stage.

1 20. (original) An apparatus according to claim 16 wherein each second stage
2 module comprises:
3 a first register having locations configured to store each bit of said output of said
4 first stage; and
5 a bank of XORs having one set of inputs from said first register and a second set
6 of inputs from the bits of input k, the output of each XOR representing one bit of said random
7 number output.

1 21. (original) An apparatus according to claim 20 wherein said M second
2 stage modules produce an approximation of the full said random number output.